



IEC 62680-4-1

Edition 1.0 2022-10

INTERNATIONAL STANDARD



**Universal Serial Bus interfaces for data and power –
Part 4-1: Universal Serial Bus 4™ Specification**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 29.200; 33.120.20; 35.200

ISBN 978-2-8322-5816-3

Warning! Make sure that you obtained this publication from an authorized distributor.

INTERNATIONAL ELECTROTECHNICAL COMMISSION

UNIVERSAL SERIAL BUS INTERFACES FOR DATA AND POWER

Part 4-1: Universal Serial Bus 4™ Specification

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62680-4-1 has been prepared by technical area 18: Multimedia home systems and applications for end-user networks, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard was prepared by the USB Implementers Forum (USB-IF). The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

The text of this International Standard is based on the following documents:

Draft	Report on voting
100/3754/CDV	100/3813/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The "colour inside" logo on the cover page of this document indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The IEC 62680 series is based on a series of specifications that were originally developed by the USB Implementers Forum (USB-IF). These specifications were submitted to the IEC under the auspices of a special agreement between the IEC and the USB-IF.

This standard is the USB-IF publication, USB4™ Specification, Version 1.0 with Errata and ECN through May 19, 2021.

The USB Implementers Forum, Inc.(USB-IF) is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. The Forum facilitates the development of high-quality compatible USB peripherals (devices), and promotes the benefits of USB and the quality of products that have passed compliance testing.

ANY USB SPECIFICATIONS ARE PROVIDED TO YOU "AS IS, "WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE USB IMPLEMENTERS FORUM AND THE AUTHORS OF ANY USB SPECIFICATIONS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OR INFORMATION IN THIS SPECIFICATION.

THE PROVISION OF ANY USB SPECIFICATIONS TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

Entering into USB Adopters Agreements may, however, allow a signing company to participate in a reciprocal, RAND-Z licensing arrangement for compliant products. For more information, please see:

<https://www.usb.org/documents>

IEC DOES NOT TAKE ANY POSITION AS TO WHETHER IT IS ADVISABLE FOR YOU TO ENTER INTO ANY USB ADOPTERS AGREEMENTS OR TO PARTICIPATE IN THE USB IMPLEMENTERS FORUM."

Universal Serial Bus 4 (USB4™) Specification

Apple Inc.

HP Inc.

Intel Corporation

Microsoft Corporation

Renesas Corporation

STMicroelectronics

Texas Instruments

Version 1.0 with Errata and ECN through May 19, 2021

May 2021

Release History

Version	Comments	Issue Date
1.0	First release	August 2019
1.0 with Errata and ECN through May 4, 2020	Includes errata and ECN through May 4, 2020 as part of the specification text.	June 2020
1.0 with Errata and ECN through October 15, 2020	Includes errata and ECN through October 15, 2020 as part of the specification text.	October 2020
1.0 with Errata and ECN through May 19, 2021	Includes errata and ECN through May 19, 2021 as part of the specification text.	May 2021

NOTE: Adopters may only use this USB specification to implement USB or third party functionality as expressly described in this Specification; all other uses are prohibited.

LIMITED COPYRIGHT LICENSE: The Promoters grant a conditional copyright license under the copyrights embodied in this USB Specification to use and reproduce the Specification for the sole purpose of, and solely to the extent necessary for, evaluating whether to implement the Specification in products that would comply with the specification. Without limiting the foregoing, use of the Specification for the purpose of filing or modifying any patent application to target the Specification or USB compliant products is not authorized. Except for this express copyright license, no other rights or licenses are granted, including without limitation any patent licenses. In order to obtain any additional intellectual property licenses or licensing commitments associated with the Specification a party must execute the USB Adopters Agreement. **NOTE:** By using the Specification, you accept these license terms on your own behalf and, in the case where you are doing this as an employee, on behalf of your employer.

INTELLECTUAL PROPERTY DISCLAIMER

THIS SPECIFICATION IS PROVIDED TO YOU “AS IS” WITH NO WARRANTIES WHATSOEVER INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE AUTHORS OF THIS SPECIFICATION DISCLAIM ALL LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO THE USE OR IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. THE PROVISION OF THIS SPECIFICATION TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

Please send comments to techsup@usb.org.

For industry information, refer to the USB Implementers Forum web page at <http://www.usb.org>.

USB Type-C®, USB-C®, USB 2.0 Type-C™, and USB4™ are trademarks of the Universal Serial Bus Implementers Forum (USB-IF). DisplayPort™ is a trademark of VESA. All product names are trademarks, registered trademarks, or service marks of their respective owners.

Thunderbolt™ is a trademark of Intel Corporation. You may only use the Thunderbolt™ trademark or logo in conjunction with products designed to this specification that complete proper certification and executing a Thunderbolt™ trademark license – see usb.org/compliance for further information

Copyright © 2021, USB Promoter Group (Apple Inc., HP Inc., Intel Corporation, Microsoft Corporation, Renesas Corporation, STMicroelectronics, and Texas Instruments).

Acknowledgement of Technical Contribution

The authors of this specification would like to recognize the following people who participated in the USB4 Specification technical work group.

Apple Inc. – Promoter Company Employees

Majd Abu Tayeh	Nimrod Agmon	Lior Aloni	Brian Baek
Omer Bar-Lev	Moshe Benyamini	Gopu Bhaskar	Carlos Calderon
David Conroy	Bill Cornelius	Scott Deandrea	William Ferry
Amit Flanter	Itay Franko	Radia Gantous	Alex Gerber
Mark Goikhman	Nir Guetta	Yair Hershkovitz	Scott Jackson
Husam Khashiboun	Alan Kobayashi	Alexei Kosut	Christine Krause
Dmitri Krichevsky	Alex Lozovik	Rachel Menes	Shlomi Mor
Shlomi Museri	Mona Omari	Tal Ostro	Arie Peled
Collin Pieper	Idan Reller	Reese Schreiber	Oleg Schtofenmaher
Etan Shirron	Ori Moshe Stern	Jose Tierno	Maxim Tsudik
Anatoly Uskach	Jeff Wilcox	Dan Wilson	Ohad Zalcman

HP Inc. – Promoter Company Employees

Roger Benson	Marcus Benzel	Alan Berkema	Kenneth Chan
Frank Chen	Phil Chen	Hosup Chung	Glen Dower
Mark Lessman	Nam Nguyen	Roger Pearson	Kenneth Smith
Chris Tabarez			

Intel Corporation – Promoter Company Employees

Nausheen Ansari	Noam Arzy	Alexandre Audier	Binata Bhattacharyya
Huimin Chen	Hengju Cheng	Salauddin Choudhury	John Crouter
Maxim Dan	Jhuda Dayan	Yoni Dishon	Eran Galil
Saranya Gopal	Venkataramani Gopalakrishnan	Raul Gutierrez	Michael Gouzenfeld
Mickey Gutman	Benjamin Hacker	Yaniv Hayat	Uri Hermoni
Alon Horn	Abdul Ismail	Abhilash K V	Ziv Kabiry
Vijaykumar Kadgi	Vijay Kasturi	Sergey Khaykin	Lev Kolomiets
Vladislav Kopzon	Efraim Kugman	Edmond Lau	Uriel Lemberger
Yun Ling	Guobin Liu	Balaji Manoharan	Liran Manor
Uma Medepalli	Assaf Mevorach	Hezi Naaman	Ohad Navon
Naod Negussie	CheeLim Nge	Leonid Plaks	Duane Quiet
Rajaram Regupathy	Reuven Rozic	Oren Salomon	Zeeshan Sarwar
Brad Saunders	Leonid Shaposhnik	Ehud Shoor	Ari Sharon

Uri Soloveychik	Einat Surijan	Aviel Uzan	Karthi Vadivelu
Alex Vekker	Chen Vrubel	Stephanie Wallick	Tzewen Wang
Sarel Wechsler	Ady Weiss	Vitaly Zhivov	Gal Yedidia
Vladimir Yudovich	Aruni Nelson		

Microsoft Corporation – Promoter Company Employees

Randy Aull	Jim Belesiu	Martin Borve	Anthony Chen
Jesse Chen	Matt Chung	Aacer Daken	Rajib Dutta
Mark Friend	Philip Froese	David Hargrove	Robbie Harris
Kit Hui	Toby Nixon	Rahul Ramadas	Andrea Severson
Kiran Shastry	Nathan Sherman	Ji Sun	Shyamal Varma

Renesas Corporation – Promoter Company Employees

Tam Do	Robert Dunstan	Philip Leung	Kiichi Muto
Ziba Nami	Hajime Nozaki	Raman Sargis	Yoshiyuki Tomoda
Starry Tsai	Jia Wei	Toshifumi Yamaoka	

STMicroelectronics – Promoter Company Employees

Nathalie Ballot	Joel Huloux	Gerard Mas	
-----------------	-------------	------------	--

Texas Instruments – Promoter Company Employees

Mike Campbell	Anant Gole	Craig Greenburg	Michael Koltun IV
Sai Karthik Rajaraman	Anwar Sadat	Cory Stewart	Sue Vining
Deric Waters	Gregory Watkins		

Contributor Company Employees

ACON, Advanced-Connectek, Inc.	Victory Chen	Conrad Choy	Vicky Chuang
	Jessica Feng	Sharon Hsiao	Wayne Wang
Advanced Micro Devices	Dennis Au	Nat Barbiero	Jason Chang
	Michael Comai	Walter Fry	Will Harris
	Jason Hawken	Jim Hunkins	Ling Kong
	Scott Ogle	Victor Salim	Joseph Scanlon
	Peter Teng		
Allion Labs, Inc.	Howard Chang	Casper Lee	Brian Shih
Analogix Semiconductor, Inc.	Greg Stewart	Haijian Sui	Yueke Tang
	Ning Zhu		
Anritsu Corporation	Wataru Aoba	John Jerico Custodio	Kazuhiro Fujinuma

	Hiroshi Goto	Alessandro Messina	Tadanori Nishikobara
	Ryo Sunayama	Toshihiro Suzuki	Mitsuhiro Usuba
	Takeshi Wada		
ASMedia Technology Inc.	Chang Chinyu	Chang Weiyun	Chen Chiahsin
	Chen Chunhung	Chuang Weber	Kuo Han Sung
	Lin Curtis	Lin ShuYu	Tseng PS
	Tseng YD	Wei Daniel	Wu ShengChung
Avery Design Systems, Inc.	Chris Browy	Chilai Huang	Zhihong Zeng
BitifEye Digital Test Solutions GmbH	Sebastian Muschala	Hermann Stehling	
Bizlink Technology, Inc.	Alex Chou	Morphy Hsieh	Kevin Tsai
Cadence Design Systems, Inc.	Marcin Behrendt	Jacek Duda	Shikha Gupta
	Gaurav Jain	Poonam Khatri	Yash Kothari
	Vinod Lakshman	Shivaji Magadum	Andy Mauffet-Smith
	Rohit Mishra	Uyen Nguyen	Raja Pounraj
	Thirumal Reddy	Anand RK	Anshul Shah
	Neelabh Singh	Ofer Steinberg	Mark Summers
	Claire Ying	Wasiq Zia	
Corigine, Inc.	Kevin Fan	Ali Khan	Xiao Xiao
Corning Optical Communications LLC	Mark Bradley	Wojciech Giziewicz	Ian McKay
	Jamie Silva		
Cypress Semiconductor	Mark Fu	Naman Jain	Savan Javia
	Palani Subbiah		
Dell Inc.	Mohammed Hijazi	Tom Lanzoni	Ken Nicholas
	Marcin Nowak	Scott Ogle	Adie Tan
	Lee Zaretsky		
Diodes Incorporated	Qun Song		
DisplayLink (UK) Ltd.	Pete Burgers	Dan Ellis	
DJI Technology Co., Ltd.	Steve Huang		
Electronics Testing Center, Taiwan	Sophia Liu		
Elka International Ltd.	Alvin Cheng	Chloe Hsieh	Roy Ting

	Jui-Ming Yang		
Ellisys	Abel Astley	Mario Pasquali	Chuck Trefts
	Tim Wei		
Etron Technology, Inc.	Andy Chen	Shihmin Hsu	Bryan Huang
	Chien-Cheng Kuo	Jen Hong Larn	
Foxconn / Hon Hai	Patrick Casher	Joe Chen	Jason Chou
	Fred Fons	Bob Hall	Terry Little
	Christine Tran	A.J. Yang	Jie Zheng
Fresco Logic Inc.	Tim Barilovits	Bob McVay	Christopher Meyers
	Jie Ni	Jeffrey Yang	
Genesys Logic, Inc.	Sean Chen	Gerry Chou	Thomas Hsieh
	Jerry Hu	Perlman Hu	Roy Huang
	ChunYen Kuo	Weddell Lee	Jimmy Lin
	Miller Lin	D.C. Lu	Greg Tu
	Han Wu	Yihsun Wu	
Google Inc.	Mark Hayter	Benson Leung	Raj Mojumder
	David Schneider		
Granite River Labs	Nikhil Acharya	Yun Han Ang	Sandy Chang
	Allen Chen	Cyan Chen	Swee Guan Chua
	Alan Chuang	Steven Lee	Caspar Lin
	Tim Lin	Krishna Murthy	Johnson Tan
	Rajaraman V	Chin Hun Yaep	
Hotron Precision Electronic Ind. Corp.	Rosa Chen	Patrick Yeh	YF Zhang
I-PEX (Dai-ichi Seiko)	Alan Kinningham	Ro Richard	
Japan Aviation Electronics Industry Ltd.	Mark Saubert	Junichi Takeuchi	
JMicron Technology Corp.	Charon Chen	Mika Cheng	Kevin Liu
Kandou Bus SA	Brian Holden	Hitaish Sharma	David Stauffer
	Andrew Stewart	Mark Vennebarger	
Keysight Technologies Inc.	Atsushi Imaoka	Biing Lin Lem	Jit Lim
	Francis Liu	Roland Scherzinger	

L&T Technology Services	Binu Chinna Thankam	Sunil Kumar	Siddharth Pethe
	Badrinath Ramachandra	Arunkumar Selvam	Gayathri SN
LeCroy Corporation	Alan Blankman	Patrick Connally	Carl Damn
	David Fraticelli	Daniel H Jacobs	Farnoosh Jafari
	Tyler Joe	Carlo Mazzetti	Mike Micheletti
	Kathryn Morales	Jeff Sabuda	Joseph Schachner
	Chris Webb		
Lenovo	Toshikazu Horino	Shinji Matsushima	Yuuki Matsuura
	Nozomu Nagata	Munefumi Nakata	Kazuya Shibayama
	Shunki Sugai	Chikara Takahashi	Masahiro Tokuno
	Kayanagi Tsuneo		
LG Electronics Inc.	Do Kyun Kim	Yoon Jong Lee	Seung Yoo
Lintes Technology Co., Ltd.	Tammy Huang	Charles Kaun	RD Lintes
	Max Lo	CT Pien	Jin Yi Tu
	Jason Yang		
Lotes Co., Ltd.	Regina Liu-Hwang	John Lynch	
Luxshare-ICT	Josue Casillo	CY Hsu	Antony Lin
	John Lin	Stone Lin	Scott Shuey
	Eric Wen	Pat Young	
Maxio Technology (Hangzhou) Ltd.	George Fang		
MediaTek Inc.	Henry Chen	Alexyc Lin	Pochou Lin
	Chiachun Wang		
MegaChips Corporation	Rahul Agarwal	Ramesh Dandapani	Satoru Kumashiro
	Ryuichi Mariizumi	Sireesha Vemulapalli	Nobu Yanagisawa
Mercedes-Benz Research & Development, North America, Inc.	Hans Wickler		
Microchip Technology Inc.	Mark Bohm	Atish Ghosh	Fernando Gonzalez
	Mark Gordon	Richard Petrie	Brigham Steele
	Anthony Tarascio	Robert Zakowicz	
Molex LLC	Alan MacDougall		
MQP Electronics Ltd.	Sten Carlsen	Pat Crowe	

Newnex Technology Corp.	Sam Liu		
NVIDIA	Jamie Aitken	Mark Overby	
NXP Semiconductors	Mahmoud El Sabbagh	Ken Jaramillo	Abhijeet Kulkarni
	Vijendra Kuroodi	Krishnan TN	
Oculus VR LLC	Marty Evans	Joaquin Fierro	Chao Hu
ON Semiconductor	Eduardo De Reza	Oscar Freitas	Christian Klein
	Amir Lahooti		
Parade Technologies, Inc.	Jian Chen	Jimmy Chiu	Mark Qu
	Craig Wiley	Paul Xu	Kevin Yuan
	Alan Yuen		
Phison Electronics Corp.	Jimmy Chen	Ko Hong Lipp	Sebastien Jean
	Stark Kuan	Thomas Lee	Anton Lin
	Winnie Lu	Wei Sui-Ning	James Tsai
	Michael Wu	Fu-Hua Yang	Chang Yuan-Cheng
Qualcomm, Inc	Tomer Ben Chen	Yiftach Benjamini	Richard Burrows
	Amit Gil	James Goel	Philip Hardy
	Raja Jagadeesan	Lalan Mishra	Dmitrii Vasilchenko
	Chris Wiesner		
Realtek Semiconductor Corp.	Chung-Chun Chen	Jen Wen Chen	Shen Chen
	Jonathan Chou	Chang Ding	Yao Feng
	Bokai Huang	An-Ming Lee	Ray Lee
	Ryan Lin	Terry Lin	Luobin Wang
	Kay Yin	Chris Zeng	
Rohde & Schwarz GmbH & Co. KG	Johannes Ganzert	Randy White	
Samsung Electronics Co., Ltd.	Jaedeok Cha	KangSeok Cho	CheolYoon Chung
	Sangju Kim	Termi Kwon	Cheolho Lee
	Edward Lee	Jun Bum Lee	Chahoon Park
	Sunggeun Yoon		
Seagate Technology LLC	Alvin Cox	Paul McParland	Michael Morgan
	Cuong Tran		
Silicon Line GmbH	Ian Jackson		

SiliConch Systems Private Limited	Kaustubh Kumar	Rakesh Polasa	Satish Anand Verkila
Softnautics LLP	Bhavesh Desai	Hetal Jariwala	Dipakkumar Modi
	Ishita Shah	Ujjwal Talati	
Spectra7 Microsystems Corp.	Alex Chow	James McGrath	
Specwerkz	Sydney Fernandes	Amanda Hosler	Diane Lenox
	Soren Petersen		
STMicroelectronics	Nathalie Ballot	Joel Huloux	Gerard Mas
Sumitomo Electric Ind., Ltd., Optical Comm. R&D Lab	Sainer Siagian	Mitsuaki Tamura	
Synaptics Inc.	Jeff Lukanc	Mark Miller	Prashant Shamarao
Synopsys, Inc.	Prishkrit Abrol	Subramaniam Aravindhan	Jeanne Cai
	Jun Cao	Morten Christiansen	Scott Guo
	Eric Huang	Joseph Juan	Venkataraman Krishnan
	Jitendra Kushwaha	Behram Minwalla	Saleem Mohammad
	Rick Schmidt	Jasjeet Singh	Mahendra Singh
	John Stonick	Zongyao Wen	Fred Yu
Tektronix, Inc.	Madhusudan Acharya	Sourabh Das	Keyur Diwan
	Mark Guenther	Abhijeet Shinde	Gary Simontom
Thine Electronics, Inc.	Shuhei Yamamoto		
Tyco Electronics Corp., a TE Connectivity Ltd. company	Simon Li	Jeff Mason	Jacky Mo
	Tommy Yu	Yuanbo Zhang	Tony Zhu
Varjo Technologies	Kai Inha		
VIA Labs, Inc.	Wayne Tseng		
VIA Technologies, Inc.	Benjamin Pan	Terrance Shih	Jay Tseng
	Fong-Jim Wang		
Weltrend Semiconductor	Chao-Chee Ku	Jeng Cheng Liu	Wayne Lo
	Ho Wen Tsai	Eric Wu	Randolph Wu
	Simon Yeh		
Western Digital	David Landsman	Larry McMillan	Rob Ryan
Wilder Technologies	Steve Bright	Zach Moore	Joe O'Brien
	Majid Shayegh		

CONTENTS

1	Introduction	41
1.1	Scope of the Document	41
1.2	USB Product Compliance	41
1.3	Document Organization	41
1.4	Design Goals	41
1.5	Related Documents	41
1.6	Conventions	42
1.6.1	Precedence	42
1.6.2	Keywords	42
1.6.2.1	Informative	42
1.6.2.2	May	42
1.6.2.3	N/A	42
1.6.2.4	Normative	42
1.6.2.5	Optional	42
1.6.2.6	Reserved	42
1.6.2.7	Shall	42
1.6.2.8	Should	43
1.6.3	Capitalization	43
1.6.4	Italic Text	43
1.6.5	Numbering	43
1.6.6	Bit, Byte, DW, and Symbol Conventions	43
1.6.7	Implementation Notes	43
1.6.8	Connection Manager Notes	43
1.6.9	Pseudocode	43
1.6.10	CRC Algorithms	44
1.6.11	FourCC	44
1.7	Reserved Values and Fields	44
1.8	Terms and Abbreviations	45
2	Architectural Overview	50
2.1	USB4 System Description	50
2.1.1	Architectural Constructs	52
2.1.1.1	Routers	52
2.1.1.2	Adapters	52
2.1.1.3	USB4 Ports and Links	52
2.1.1.4	USB4 Devices	53
2.1.1.5	USB4 Host	54
2.1.1.6	Re-timers	55
2.1.1.7	Connection Manager	55
2.1.2	USB4 Mechanical	55
2.1.3	USB4 Power	55
2.1.4	USB4 System Configuration	55
2.1.5	Thunderbolt™ 3 (TBT3) Compatibility Support	55
2.1.6	USB Type-C Alternate Mode Compatibility Support	56
2.2	USB4 Fabric Architecture	56
2.2.1	USB4 Functional Stack	56

- 2.2.1.1 Electrical Layer.....57
- 2.2.1.2 Logical Layer.....57
- 2.2.1.3 Transport Layer.....57
- 2.2.1.4 Configuration Layer.....58
- 2.2.1.5 Protocol Adapter Layer.....58
- 2.2.2 USB4 Fabric Topology.....58
- 2.2.3 Paths.....59
- 2.2.4 Communication Constructs.....61
 - 2.2.4.1 USB4 Link.....61
 - 2.2.4.2 Sideband Channel.....62
- 2.2.5 USB4 Host-to-Host Communications.....63
- 2.2.6 Programming Model.....63
 - 2.2.6.1 Connection Manager.....63
 - 2.2.6.2 Configuration Spaces.....64
 - 2.2.6.3 Operations.....64
- 2.2.7 Time Synchronization.....64
- 2.2.8 USB4 Fabric Data Integrity.....64
- 2.2.9 Global Life of a Router.....65
- 2.2.10 Protocol Tunneling.....65
 - 2.2.10.1 USB3 Tunneling.....66
 - 2.2.10.2 Display Tunneling.....70
 - 2.2.10.3 PCIe Tunneling.....73
 - 2.2.10.4 Host Interface Adapter.....77
- 3 Electrical Layer.....79
 - 3.1 Sideband Channel Electrical Specifications.....80
 - 3.2 USB4 Ecosystem.....81
 - 3.2.1 Insertion-Loss Considerations (Informative).....81
 - 3.2.2 Coded Bit-Error-Ratio Considerations (Informative).....82
 - 3.3 USB4 Electrical Compliance Methodology.....82
 - 3.3.1 System Compliance Test Point Definitions.....82
 - 3.3.2 AC Coupling Capacitors.....83
 - 3.3.3 Reference Clock-and-Data-Recovery (CDR) Function.....84
 - 3.3.4 Reference Equalization Function.....84
 - 3.3.4.1 Reference CTLE.....85
 - 3.3.4.2 Reference DFE.....87
 - 3.3.5 Time Domain Measurements.....87
 - 3.3.6 Compliance Boards.....87
 - 3.3.6.1 Compliance Plug Test Board.....87
 - 3.3.6.2 Compliance Receptacle Test Board.....87
 - 3.4 Router Assembly Transmitter Compliance.....87
 - 3.4.1 Transmitter Specifications Applied for All Speeds.....87
 - 3.4.1.1 Transmitter Frequency Variations during Link Training....89
 - 3.4.1.2 Transmitter Differential Return Loss.....90
 - 3.4.1.3 Transmitter Common Mode Return Loss.....91
 - 3.4.1.4 Transmit Equalization.....92
 - 3.4.2 Transmitter Compliance Specifications for Gen 2.....95
 - 3.4.3 Transmitter Compliance Specifications for Gen 3 Interconnects.....97
 - 3.5 Router Assembly Receiver Compliance.....98

3.5.1	Receiver Specifications Applied for All Speeds	98
3.5.1.1	Receiver Differential Return Loss	99
3.5.1.2	Receiver Common Mode Return Loss	100
3.5.2	Receiver Uncoded BER Tolerance Testing	101
3.5.3	Receiver Multi Error-Bursts Testing	103
3.6	Captive Device Compliance	105
3.6.1	Captive Device Compliance Test Setup	105
3.6.2	Captive Device Transmitter Specifications	105
3.6.2.1	Conducted Energy in Wireless Bands	105
3.6.2.2	Transmitter Specifications	106
3.6.2.3	Transmitter Differential Return Loss	109
3.6.2.4	Transmitter Common Mode Return Loss	109
3.6.2.5	Transmit Equalization	109
3.6.3	Captive Device Receiver Specifications	109
3.6.3.1	Receiver Specifications Applied for All Speeds	109
3.6.3.2	Receiver Differential Return Loss	110
3.6.3.3	Receiver Common Mode Return Loss	110
3.6.4	Captive Device Receiver Uncoded BER Tolerance Testing	111
3.6.5	Captive Device Receiver Multi Error-Bursts Testing	112
3.7	Low Frequency Periodic Signaling (LFPS)	113
3.7.1	LFPS Signal Definition	113
3.8	Receiver Lane Margining (Testability)	114
3.8.1	Background	114
3.8.1.1	Software Margining Mode	115
3.8.1.2	Hardware Margining Mode	115
3.8.2	Receiver Voltage Margining and Timing Margining Requirements	116
3.8.3	Receiver Parameter Access	118
4	Logical Layer	119
4.1	Sideband Channel	119
4.1.1	Transactions	120
4.1.1.1	Symbols	120
4.1.1.2	Transaction Types	120
4.1.1.3	SB Register Space	128
4.1.2	Lane Initialization	136
4.1.2.1	Phase 1 – Determination of Initial Conditions	137
4.1.2.2	Phase 2 – Router Detection	139
4.1.2.3	Phase 3 – Determination of USB4 Port Characteristics ..	139
4.1.2.4	Phase 4 – Lane Parameters Synchronization and Transmit Start	140
4.1.2.5	Phase 5 – Link Equalization	140
4.2	Logical Layer State Machine	143
4.2.1	Lane Adapter State Machine	143
4.2.1.1	Disabled	144
4.2.1.2	CLd	144
4.2.1.3	Training	145
4.2.1.4	CL0	152
4.2.1.5	Lane Bonding	153
4.2.1.6	Low Power (CL0s, CL1, and CL2)	154

- 4.2.2 USB4 Link Transitions 170
 - 4.2.2.1 Transition from One Single-Lane Link to Two Single-Lane Links..... 170
 - 4.2.2.2 Transition from Two Single-Lane Links to Dual-Lane Link 171
 - 4.2.2.3 Transition from Dual-Lane Link to Two Single-Lane Links 172
 - 4.2.2.4 Transition from Two Single-Lane Links to One Single-Lane Link 172
- 4.2.3 Logical Layer Link State 173
- 4.3 USB4 Link Encoding 173
 - 4.3.1 Lane Distribution 175
 - 4.3.2 Symbol Encoding 176
 - 4.3.2.1 Symbol Encoding of Transport Layer Bytes..... 176
 - 4.3.3 Ordered Sets..... 177
 - 4.3.4 Bit Swap..... 178
 - 4.3.4.1 Sync Bits 178
 - 4.3.4.2 Data Symbol Payload 178
 - 4.3.4.3 Ordered Set Symbol Payload..... 179
 - 4.3.5 Scrambling 180
 - 4.3.6 RS-FEC..... 181
 - 4.3.6.1 RS-FEC Activation and Deactivation..... 183
 - 4.3.6.2 Pre-Coding 184
- 4.4 USB4 Link Operation 184
 - 4.4.1 Start of Data..... 184
 - 4.4.2 Error Cases and Recovery 184
 - 4.4.3 Clock Compensation and SKIP 186
 - 4.4.4 Dual-Lane Skew 186
 - 4.4.5 Disconnect 187
 - 4.4.5.1 Upstream Facing Port Disconnect..... 187
 - 4.4.5.2 Downstream Port Disconnect..... 188
 - 4.4.6 Lane Adapter Disable and Enable 190
 - 4.4.6.1 Disabled Adapter is the Upstream Adapter 191
 - 4.4.6.2 Disabled Adapter is not the Upstream Adapter..... 192
 - 4.4.7 Time Sync Notification Ordered Set (TSNOS)..... 194
- 4.5 Sleep and Wake 194
 - 4.5.1 Entry to Sleep 194
 - 4.5.2 Behavior in Sleep State 196
 - 4.5.3 Wake Events 196
 - 4.5.4 Exit from Sleep..... 197
 - 4.5.4.1 Upstream Facing Port Disconnect..... 197
 - 4.5.4.2 Wake on USB4 Event 197
- 4.6 Timing Parameters 198
- 5 Transport Layer 201
 - 5.1 Transport Layer Packets..... 201
 - 5.1.1 Bit/Byte Conventions 201
 - 5.1.2 Format 202
 - 5.1.2.1 Header 202
 - 5.1.2.2 Payload Padding 203

5.1.2.3	Error Correction Code (ECC)	204
5.1.3	Transport Layer Packets	204
5.1.3.1	Tunneled Packets	204
5.1.3.2	Control Packets	204
5.1.3.3	Link Management Packets	204
5.1.4	Effect of Link State on Transport Layer Packets	207
5.1.5	Minimum Headers Gap	208
5.2	Routing.....	209
5.2.1	Adapter Numbering Rules	209
5.2.2	HopID Rules.....	210
5.2.3	Routing Tables	211
5.2.4	Routing Rules	212
5.2.4.1	Control Packets	212
5.2.4.2	Link Management Packets	212
5.2.4.3	Tunneled Packets	213
5.2.4.4	Routing Example	213
5.2.5	Connectivity Rules	214
5.3	Quality of Service (QOS)	215
5.3.1	Packet Ordering	215
5.3.2	Flow Control.....	215
5.3.2.1	Ingress Adapter	216
5.3.2.2	Egress Adapter.....	221
5.3.2.3	Credit Counter Synchronization	223
5.3.3	Bandwidth Arbitration and Priority	223
5.3.3.1	Scheduling	224
5.3.4	Packet Forwarding Delay Jitter.....	225
5.4	Path Tear-down.....	225
5.4.1	Egress Adapter	225
5.4.2	Ingress Adapter.....	226
5.5	Timing Parameters	226
6	Configuration Layer.....	227
6.1	Domain Topology	227
6.2	Router Addressing.....	227
6.3	Router States	229
6.3.1	Uninitialized Unplugged State	230
6.3.2	Uninitialized Plugged State	230
6.3.3	Sleep State	230
6.3.4	Enumerated State	230
6.4	Control Packet Protocol	231
6.4.1	Control Adapter.....	231
6.4.2	Control Packets.....	231
6.4.2.1	Bit/Byte Conventions	231
6.4.2.2	Format.....	231
6.4.2.3	Read Request.....	232
6.4.2.4	Read Response	233
6.4.2.5	Write Request.....	235
6.4.2.6	Write Response	236
6.4.2.7	Notification Packet.....	237

- 6.4.2.8 Notification Acknowledgement Packet.....238
- 6.4.2.9 Hot Plug Event Packet.....239
- 6.4.2.10 Inter-Domain Request.....240
- 6.4.2.11 Inter-Domain Response241
- 6.4.3 Control Packet Routing242
 - 6.4.3.1 Upstream-Bound Packets242
 - 6.4.3.2 Downstream-Bound Packets.....242
 - 6.4.3.3 Processing of Read and Write Requests244
- 6.4.4 Control Packet Reliability245
- 6.5 Notification Events.....246
- 6.6 Notification Acknowledgement.....247
- 6.7 Router Enumeration.....247
- 6.8 Hot Plug and Hot Unplug Events.....249
 - 6.8.1 Router Hot Plug.....251
 - 6.8.1.1 Enumerated Routers251
 - 6.8.1.2 Uninitialized Routers.....251
 - 6.8.1.3 Hot Plugged Router251
 - 6.8.2 Router Hot Unplug.....251
 - 6.8.2.1 Hot Unplug on the Upstream Facing Port.....251
 - 6.8.2.2 Hot Unplug on a Downstream Facing Port252
- 6.9 Downstream Facing Port Reset252
- 6.10 Timing Parameters252
- 7 Time Synchronization.....253
 - 7.1 Time Synchronization Architecture253
 - 7.1.1 Synchronization Hierarchy.....253
 - 7.1.1.1 Intra-Domain Hierarchy.....253
 - 7.1.1.2 Inter-Domain Hierarchy.....254
 - 7.1.2 Time Sync Parameters254
 - 7.1.2.1 Local Time.....254
 - 7.1.2.2 Time Offset.....255
 - 7.1.2.3 Frequency Offset255
 - 7.2 Time Stamp Measurement.....256
 - 7.2.1 Asymmetry Corrections256
 - 7.3 Time Sync Protocol257
 - 7.3.1 Time Sync Handshake.....257
 - 7.3.1.1 Bi-Directional Time Sync Handshake258
 - 7.3.1.2 Uni-Directional Time Sync Handshake262
 - 7.3.2 Inter-Domain Time Sync.....264
 - 7.3.3 Packet Formats266
 - 7.3.3.1 Time Sync Notification Ordered Set Format266
 - 7.3.3.2 Follow-Up Packet Format.....266
 - 7.3.3.3 Inter-Domain Time Stamp Packet268
 - 7.4 Time Computations.....269
 - 7.4.1 Intra-Domain Equations.....271
 - 7.4.2 Inter-Domain Equations.....273
 - 7.4.2.1 Inter-Domain Time Stamp Computation274
 - 7.4.2.2 Inter-Domain Frequency Offset Computation.274
 - 7.4.2.3 Inter-Domain Time Offset Computation275

7.4.2.4	Inter-Domain Host Router Time Computation.....	276
7.4.3	Filtering.....	277
7.5	Time Synchronization Accuracy Requirements	278
7.5.1	Paired Measurement	278
7.5.2	Standalone Measurement.....	278
7.5.3	Measuring Method.....	279
7.5.4	Accuracy Parameters	280
7.6	Software Configuration	281
7.6.1	Intra-Domain Time Synchronization Setup.....	281
7.6.2	Inter-Domain Time Synchronization Setup.....	281
7.6.3	Post Time Mechanism	281
7.6.4	Time Disruption Bit.....	282
8	Configuration Spaces	283
8.1	Configuration Fields Access Types	283
8.2	Configuration Spaces	284
8.2.1	Router Configuration Space	284
8.2.1.1	Basic Configuration Registers.....	286
8.2.1.2	TMU Router Configuration Capability.....	293
8.2.1.3	Vendor Specific Capability (VSC).....	300
8.2.1.4	Vendor Specific Extended Capability (VSEC).....	301
8.2.2	Adapter Configuration Space.....	302
8.2.2.1	Basic Configuration Registers.....	304
8.2.2.2	TMU Adapter Configuration Capability	308
8.2.2.3	Lane Adapter Configuration Capability	310
8.2.2.4	USB4 Port Capability	314
8.2.2.5	USB3 Adapter Configuration Capability	320
8.2.2.6	DP Adapter Configuration Capability.....	323
8.2.2.7	PCIe Adapter Configuration Capability.....	335
8.2.3	Path Configuration Space.....	336
8.2.3.1	Path 0 Entry	336
8.2.3.2	Lane Adapters	337
8.2.3.3	Protocol Adapters	339
8.2.3.4	Path Configuration Space Access	341
8.2.4	Counters Configuration Space.....	342
8.3	Operations.....	344
8.3.1	Router Operations	344
8.3.1.1	DP Tunneling Operations.....	345
8.3.1.2	NVM Operations	348
8.3.1.3	Router Discovery Operations	353
8.3.1.4	Port Control Operations	359
8.3.2	Port Operations	360
8.3.2.1	Compliance Port Operations	362
8.3.2.2	Service Port Operations.....	372
8.3.2.3	Receiver Lane Margining Port Operations.....	373
9	USB3 Tunneling	383
9.1	USB3 Adapter Layer.....	384
9.1.1	Encapsulation	384
9.1.1.1	LFPS Encapsulation	385

9.1.1.2	Ordered Set Encapsulation	388
9.1.1.3	Link Command Encapsulation	390
9.1.1.4	Idle Symbols	390
9.1.1.5	LMP Encapsulation	390
9.1.1.6	TP Encapsulation	391
9.1.1.7	ITP Encapsulation	391
9.1.1.8	Data Packet (DP) Encapsulation	392
9.1.2	Bandwidth Negotiation	394
9.1.3	Timing Parameters	396
9.2	Internal USB3 Device	396
9.2.1	Link Layer	397
9.2.1.1	Link Training and Status State Machine (LTSSM)	397
9.2.1.2	Timers and Timeouts	397
9.2.2	USB3 Protocol Layer	398
9.2.3	Descriptors	398
9.3	Paths	398
9.3.1	Path Setup	398
9.3.2	Path Teardown	398
10	DisplayPort™ Tunneling	400
10.1	DP Adapter Protocol Stack	400
10.1.1	Transport Layer	401
10.1.2	Protocol Adapter Layer	401
10.1.3	DP Physical Layer	401
10.2	DP Adapter States	401
10.2.1	Reset	402
10.2.2	Present	402
10.2.3	Plugged	403
10.2.4	Paired	403
10.3	Interfaces	403
10.3.1	DisplayPort	403
10.3.1.1	LTTPR Non-Transparent	404
10.3.1.2	Non-LTTPR	404
10.3.1.3	LTTPR Transparent	405
10.3.2	Programming Model	405
10.3.2.1	Adapter Configuration Space	405
10.3.2.2	Path Configuration Space	405
10.3.3	Hot Plug and Hot Removal Events	406
10.3.3.1	DP OUT Adapters	406
10.3.3.2	DP IN Adapters	406
10.3.4	DisplayPort Over USB4 Fabric	408
10.3.4.1	DisplayPort Data Packet Types	408
10.3.4.2	AUX Path Packet	408
10.3.4.3	Main-Link Path Packet Formats	415
10.4	System Flows	415
10.4.1	Connection Manager Discovery	415
10.4.2	Path Configuration	416
10.4.2.1	Setup	416
10.4.2.2	Tear-down	418

10.4.3	HPD Event Propagation.....	419
10.4.3.1	HPD Plug.....	419
10.4.3.2	HPD Unplug.....	419
10.4.3.3	IRQ.....	419
10.4.3.4	HPD Delay Requirements	420
10.4.3.5	Manual HPD Control	420
10.4.4	AUX Request and Response Handling.....	420
10.4.4.1	LTTTPR Non-Transparent Mode	420
10.4.4.2	Non-LTTTPR Mode	422
10.4.4.3	LTTTPR Transparent Mode.....	425
10.4.4.4	AUX Delay Requirements	427
10.4.4.5	Aggregated DisplayPort Capabilities	427
10.4.4.6	DPCD DP Tunneling over USB4	428
10.4.5	DP Adapters Init Flow.....	429
10.4.5.1	Multi-Function DP	429
10.4.6	Source Discovery	429
10.4.6.1	LTTTPR Recognition and Modes Change	430
10.4.6.2	DPRX Capabilities Read	430
10.4.6.3	Sink Count Read	431
10.4.7	Down-Spread Control	431
10.4.8	Stream Mode Set	431
10.4.9	DSC and FEC Enable.....	431
10.4.10	DP Link Training.....	432
10.4.10.1	LTTTPR.....	432
10.4.10.2	Non-LTTTPR and LTTTPR Transparent	437
10.4.10.3	Transition to High Speed Tunnel.....	439
10.4.11	Power States Set	439
10.4.12	DP Main-Link Disable.....	439
10.4.13	Link-Init.....	440
10.4.14	DP PHY Testability.....	440
10.4.14.1	DP IN Adapter PHY Layer Testing	440
10.4.14.2	DP OUT Adapter PHY Layer Testing.....	441
10.5	High Speed Tunneling	441
10.5.1	SST Tunneling	442
10.5.1.1	Video Data Packet.....	442
10.5.1.2	Main Stream Attribute Packet	448
10.5.1.3	Blank Start Packet.....	449
10.5.1.4	Secondary Data Packet	451
10.5.1.5	Fill Count.....	455
10.5.2	MST Tunneling.....	458
10.5.2.1	Sub-MTP TU.....	458
10.5.2.2	MTP to Sub-MTP TU Examples	464
10.5.2.3	MST Packet Format.....	466
10.5.2.4	MST Packets to DP MTP	467
10.5.3	FEC	467
10.5.3.1	SR Count.....	467
10.5.3.2	DP IN Adapter Requirements.....	468
10.5.3.3	DP OUT Adapter Requirements	468

10.5.3.4	FEC_DECODE Packet	469
10.5.4	DP OUT Adapter Buffer	469
10.5.4.1	Buffer Operation	470
10.5.4.2	Accumulation Cycles	470
10.5.5	HDCP	471
10.6	DP Link Clock Sync	471
10.6.1	Synchronization Method	472
10.6.1.1	Events	472
10.6.1.2	Lifetime Counter	472
10.6.1.3	DP Clock Sync Packet	474
10.6.2	DP Adapter Requirements	476
10.6.2.1	DP IN Adapter Requirements	476
10.6.2.2	DP OUT Adapter Requirements	476
10.7	DP BW Allocation Mode	477
10.7.1	DP BW Allocation Mode Enablement	477
10.7.2	Interaction with DPTX	478
10.7.2.1	Estimated Bandwidth	481
10.7.3	Interaction with the Connection Manager	481
10.8	Timing Parameters	483
11	PCI Express Tunneling	484
11.1	PCIe Adapter Layer	485
11.1.1	Encapsulation	485
11.1.1.1	PCIe TLP and DLLP	485
11.1.1.2	PCIe Ordered Sets	489
11.1.1.3	Electrical Idle State	491
11.1.1.4	PERST	491
11.1.2	USB4 Hot-Plug	492
11.2	Internal PCIe Ports	492
11.2.1	PCIe Physical Layer Logical Sub-block	492
11.2.1.1	Encoding	492
11.2.1.2	Link Training and Status State Machine (LTSSM)	492
11.2.1.3	ASPM L1 Entry	493
11.2.1.4	Clock Tolerance Compensation	493
11.2.1.5	Compliance Mode	493
11.2.1.6	Clock Power Management	493
11.2.1.7	L2 State	493
11.2.2	PCIe Data Link Layer	493
11.2.3	PCIe Transaction Layer	493
11.2.4	PCIe Link Timers (Informative)	494
11.2.5	Precision Time Measurement (PTM) Mechanism	495
11.2.5.1	Parameter Generator	497
11.2.5.2	Parameter Consumer	497
11.2.5.3	PTM Calculations	498
11.2.6	Timing Parameters	500
11.3	Paths	500
11.3.1	Path Set-Up	500
11.3.2	Path Tear-Down	500
12	Host Interface	501

12.1	Descriptor Ring Mode	502
12.1.1	DW, Byte, and Bit Order	502
12.1.2	Raw Mode	503
12.1.3	Frame Mode	503
12.2	End-to-End (E2E) Flow Control	505
12.2.1	E2E Flow Control Packets	505
12.2.1.1	E2E Credit Grant Packet	505
12.2.1.2	E2E Credit Sync Packet	507
12.2.2	Flow Control Rules	507
12.2.2.1	Credit Update	507
12.2.2.2	Credit Counter Synchronization	507
12.2.2.3	Transmitting Host Interface Rules	508
12.2.2.4	Receiving Host Interface Rules	509
12.3	Transmit Interface	510
12.3.1	Transmit Descriptor Structure	510
12.3.2	Transmit Flow	511
12.3.2.1	Frame Mode	511
12.3.2.2	Raw Mode	512
12.4	Receive Interface	513
12.4.1	Receive Descriptor Structure	513
12.4.2	Receive Flow	515
12.4.2.1	Frame Mode	515
12.4.2.2	Raw Mode	516
12.5	Interrupts	517
12.5.1	Interrupt Causes	517
12.5.2	Interrupt Masks	517
12.5.3	Interrupt Vectors	517
12.5.4	Interrupt Moderation	517
12.6	Programming Interface	518
12.6.1	Access Types	519
12.6.2	Registers Summary	519
12.6.3	Registers Description	520
12.6.3.1	Host Interface Control	520
12.6.3.2	Transmit Descriptor Rings	522
12.6.3.3	Receive Descriptor Rings	524
12.6.3.4	Interrupts	527
12.7	Timing Parameters	532
13	Interoperability with Thunderbolt™ 3 (TBT3) Systems	532
13.1	Electrical Layer	532
13.2	Logical Layer	533
13.2.1	Sideband Channel	533
13.2.1.1	Bidirectional Re-timer	533
13.2.1.2	Transactions	533
13.2.1.3	SB Register Space	536
13.2.1.4	Lane Initialization	536
13.2.2	Logical Layer State Machine	541
13.2.2.1	CLd State	541
13.2.2.2	TS1 and TS2 Ordered Sets	542

- 13.2.2.3 Low Power (CL0s, CL1, and CL2) 542
- 13.2.3 USB4 Link Operation 542
 - 13.2.3.1 USB4 Link Transitions 542
 - 13.2.3.2 Pre-Coding 542
- 13.2.4 Sleep and Wake 542
 - 13.2.4.1 Entry to Sleep 542
 - 13.2.4.2 Behavior in Sleep State 543
 - 13.2.4.3 Wake Events 543
 - 13.2.4.4 Exit from Sleep 543
- 13.2.5 Timing Parameters 544
- 13.3 Transport Layer 544
 - 13.3.1 Adapter Numbering Rules 544
 - 13.3.2 Maximum HopID 544
 - 13.3.3 Connectivity Rules 544
 - 13.3.4 Buffer Allocation 545
- 13.4 Configuration Layer 545
 - 13.4.1 Router Enumeration 545
 - 13.4.2 Notification Packet 545
 - 13.4.3 Bit Banging Interface 545
 - 13.4.4 Control Packet Routing 546
 - 13.4.4.1 Downstream-Bound Packets 546
 - 13.4.4.2 Uninitialized Router Flow 547
- 13.5 Time Synchronization 547
- 13.6 Configuration Spaces 547
 - 13.6.1 Router Configuration Space 548
 - 13.6.1.1 Vendor Specific 1 Capability 548
 - 13.6.1.2 Vendor Specific 3 Capability 552
 - 13.6.1.3 Vendor Specific 4 Capability 555
 - 13.6.1.4 Vendor Specific Extended 6 Capability 556
 - 13.6.2 Adapter Configuration Space 563
 - 13.6.2.1 Basic Attributes 563
 - 13.6.2.2 USB4 Port Capability 564
- 13.7 PCI Express Tunneling 564
 - 13.7.1 PCIe Power Management 564
 - 13.7.1.1 L1 564
 - 13.7.1.2 L2 565
- 13.8 DisplayPort Tunneling 565
 - 13.8.1 AUX Handling 565
 - 13.8.1.1 DP IN Adapter Requirements 565
 - 13.8.1.2 DP OUT Adapter Requirements 565
 - 13.8.2 IRQ Handling 566
 - 13.8.3 Connection Manager Discovery 566
 - 13.8.3.1 TBT3 Connection Manager 566
 - 13.8.3.2 TBT3 Router Discovery 566
 - 13.8.4 Sink Count Read 567
 - 13.8.5 Power States Set 567
 - 13.8.6 DisplayPort Link Training 567
 - 13.8.6.1 DP IN Adapter Requirements 568

13.8.6.2 DP OUT Adapter Requirements	569
13.9 USB3 Functionality	570
13.10 Host-to-Host Tunneling	572
A Verification of CRC, Scrambling, and FEC Calculations	572
A.1 Transport Layer Packet HEC	572
A.2 Control Packet CRC	572
A.3 Sideband Channel AT Transaction CRC	573
A.4 Scrambler	574
A.5 Logical Layer RS-FEC	574
A.6 USB3 Tunneling CRC	579
A.7 Host Interface Frame CRC	580
A.8 ECC Examples	585
B Summary of Transport Layer Packets	586
C Examples of Link Power Management Flows	587
C.1 Entry to Low Power States	587
C.1.1 Successful Entry to CL2 State	587
C.1.2 Successful Entry to CL0s State	588
C.1.3 Rejection to Enter CL2 State	589
C.1.4 Concurrent Requests to Enter Low Power State	589
C.1.5 CL2_REQ Ordered Sets are Not Received	590
C.1.6 CL2_REQ Ordered Sets are Partially Received	591
C.1.7 Error in CL2_ACK Ordered Sets	592
C.1.8 Error in CL_OFF Ordered Sets	593
C.2 Exit from Low Power States	594
C.2.1 Example: Exit from CL0s State	594
C.2.2 Example: Exit from CL2 (or CL1) State	596
D Serial Time Link Protocol (STLP)	598
D.1 Time Synchronization	598
D.2 Serial Time Link Packet Format	599
D.3 TMU_CLK_OUT and TMU_CLK_IN	602
E Ingress Buffer Space	603
E.1 Target Bandwidth Buffer Calculation	603
E.1.1 Example for USB3 Tunneling Ingress Buffer Calculation	603
E.2 Ingress Buffers Calculation for DP Main Path	604

Figures

Figure 2-1. USB4/USB3.2 Dual Bus System Architecture	51
Figure 2-2. Single-Lane USB4 Link	53
Figure 2-3. Dual-Lane USB4 Link	53
Figure 2-4. Example of a USB4-Based Dock	54
Figure 2-5. USB4 Functional Stack Layers	56
Figure 2-6. USB4 Port (Lane Adapter), Protocol Adapter and Control Adapter across Functional Layers	57
Figure 2-7. Example USB4 Physical Topology (No Loop) and Spanning Tree	58
Figure 2-8. Example USB4 Physical Topology (with Loop) and Spanning Tree	59

Figure 2-9. Paths across a USB4 Fabric	60
Figure 2-10. USB4 Communication by Functional Layer	61
Figure 2-11. Example Control Packet Traversing Several Routers	62
Figure 2-12. Example USB4 Host-to-Host Connections.....	63
Figure 2-13 Example of a USB4 Host with USB3 Tunneling Highlighted	66
Figure 2-14. Example of a USB4 Hub with USB3 Tunneling Highlighted	67
Figure 2-15. Example of a USB4 Peripheral Device with USB3 Tunneling Highlighted	67
Figure 2-16. Protocol Stack for USB3 Tunneling	68
Figure 2-17. Example of a USB4 Fabric with USB3 Tunneling	69
Figure 2-18. Protocol Stacks along a USB3 Tunnel	70
Figure 2-19. Example Topology for DisplayPort Tunneling.....	70
Figure 2-20. DP IN and OUT Protocol Adapters in LTTTPR Non-Transparent and LTTTPR Transparent Modes.....	71
Figure 2-21. DP IN and OUT Protocol Adapters in Non-LTTTPR Mode	72
Figure 2-22. Protocol Stacks along a DisplayPort Tunneled Path.....	73
Figure 2-23. Example Structure of a USB4 Host with PCIe Tunneling Highlighted.....	74
Figure 2-24. Example USB4 Hub with PCIe Tunneling Highlighted	74
Figure 2-25. Example USB4 Device with PCIe Tunneling Highlighted	75
Figure 2-26. Protocol Stack for PCIe Tunneling	75
Figure 2-27. Example of a USB4 Fabric with PCIe Tunneling.....	76
Figure 2-28. Protocol Stacks along a PCIe Tunnel.....	77
Figure 2-29. Protocol Stacks along a Path between Hosts	78
Figure 2-30. Descriptor Ring and Data Buffers	79
Figure 3-1. Combined Forward-Error-Correction and Pre-Coding Scheme	82
Figure 3-2. Compliance Points Definition	83
Figure 3-3. Examples for AC-Coupling Capacitor Placement	83
Figure 3-4. Jitter Transfer Function	84
Figure 3-5. Reference Receiver Equalization.....	85
Figure 3-6. Frequency Response of Gen 2 Reference CTLE.....	86
Figure 3-7. Frequency Response of Gen 3 Reference CTLE.....	86
Figure 3-8. Router Assembly Transmitter Frequency Variation During Training.....	90
Figure 3-9. Example Transmitter Frequency During Steady-State.....	90
Figure 3-10. TX Differential Return Loss Mask	91
Figure 3-11. TX Common-Mode Return Loss Mask.....	92
Figure 3-12. Transmitter Equalizer Structure	93
Figure 3-13. Transmitter Equalization Frequency Response for Gen 2 Systems	94
Figure 3-14. Transmitter Equalization Frequency Response for Gen 3 Systems	95
Figure 3-15. TX Mask Notations	97
Figure 3-16. RX Differential Return-Loss Mask.....	100
Figure 3-17. RX Common Mode Return-Loss Mask	101
Figure 3-18. Receiver Tolerance Test Topologies.....	102
Figure 3-19. Receiver Tolerance Test Setups	102

Figure 3-20. Captive Device Compliance Test Setup	105
Figure 3-21. Captive Device Receiver Test Setup	112
Figure 3-22. Signaling During Power Management State Exit	114
Figure 3-23. Software Margining Mode Example	115
Figure 3-24. Hardware Margining Flow	116
Figure 3-25. RX Margining Range Requirements	117
Figure 3-26. Optional RX Margining Range Capabilities	118
Figure 4-1. Cable Topologies (Informative)	120
Figure 4-2. Symbol and Bit Order on Sideband Channel	121
Figure 4-3. Propagation of a Broadcast RT Transaction	124
Figure 4-4. Sideband Channel Receive Transaction State Machine	127
Figure 4-5. Overview of Lane Initialization	137
Figure 4-6. Example of Lane Reversal	138
Figure 4-7. Progression of Link Equalization	141
Figure 4-8. The Lane Adapter State Machine	143
Figure 4-9. Training Sub-State Machine	145
Figure 4-10. Lane Bonding Sub-State Machine	153
Figure 4-11. Structure of a CL_WAKE1.X Ordered Set Symbol	157
Figure 4-12. Packet Flow in the Logical Layer	174
Figure 4-13. Byte Transmission Order on Lanes	175
Figure 4-14. Byte Ordering of Transport Layer Packets to the Logical Layer	176
Figure 4-15. Byte Ordering of Idle Packets to the Logical Layer	176
Figure 4-16. Symbol Encoding of Data Symbols	177
Figure 4-17. Symbol Encoding of Ordered Set Symbols	178
Figure 4-18. Bit and Byte Ordering on the Wire – Data Symbol Payload	179
Figure 4-19. Bit and Byte Ordering on the Wire – Ordered Set Symbol Payload	180
Figure 4-20. RS-FEC Data Structures	183
Figure 4-21. Lane Disable of the Upstream Adapter	192
Figure 4-22. Lane Disable Flow	193
Figure 5-1. Convention for Transport Layer Diagrams	202
Figure 5-2. Transport Layer Packet Format	202
Figure 5-3. Idle Packet Contents	205
Figure 5-4. Credit Grant Packet Format	206
Figure 5-5. Path Credit Sync Packet Format	206
Figure 5-6. Shared Buffers Credit Sync Packet Format	207
Figure 5-7. Two Concurrent Data Symbols Example	209
Figure 5-8. Routing Table	212
Figure 5-9. Routing Example	214
Figure 5-10. Example of Connectivity for USB3 Adapters	215
Figure 5-11. Egress Adapter Scheduler	224
Figure 6-1. Example of TopologyID Assignment	228
Figure 6-2. Host Router State Machine	229

Figure 6-3. Device Router State Machine	229
Figure 6-4 Control Packet Format.....	231
Figure 6-5. Route String Format	232
Figure 6-6. Read Request.....	233
Figure 6-7. Read Response.....	235
Figure 6-8. Write Request.....	236
Figure 6-9. Write Response	237
Figure 6-10. Notification Packet.....	238
Figure 6-11. Notification Acknowledgement Packet	239
Figure 6-12. Hot Plug Event Packet.....	240
Figure 6-13. Inter-Domain Request.....	241
Figure 6-14. Inter-Domain Response	242
Figure 6-15. Example of Control Packet Routing Between Domains.....	244
Figure 7-1. Time Synchronization Hierarchy within a Domain (Informative).....	254
Figure 7-2. Local Time Counter Format	255
Figure 7-3. <i>TimeOffsetFromHR</i> Register Format.....	255
Figure 7-4. <i>FreqOffsetFromHR</i> Register Format	256
Figure 7-5. <i>Time Measurement Model for 64/66b Encoding</i>	256
Figure 7-6. Bi-Directional Time Sync Handshake.....	258
Figure 7-7. UFP State Machine for Bi-Directional Time Sync Handshake (Recommended).....	260
Figure 7-8. DFP State Machine for Bi-Directional Time Sync Handshake (Recommended).....	261
Figure 7-9. Uni-Directional Time Sync Handshake.....	262
Figure 7-10. DFP State Machine for Uni-Directional Time Sync Handshake (Recommended).....	263
Figure 7-11. UFP State Machine for Uni-Directional Time Sync Handshake (Recommended).....	264
Figure 7-12. Inter-Domain Time Sync Protocol (Informative).....	266
Figure 7-13. Follow-Up Packet Format	267
Figure 7-14. Inter-Domain Time Stamp Packet Format	269
Figure 7-15. Inter-Domain Topology (Informative).....	271
Figure 7-16. Filter Attenuation.....	277
Figure 7-17. Dynamic Noise Types	278
Figure 7-18. Standalone Measurement Points	279
Figure 7-19. Time Events	280
Figure 7-20. Measuring Method.....	280
Figure 8-1. Structure of the Router Configuration Space.....	285
Figure 8-2. UUID Format	293
Figure 8-3. Structure of the TMU Router Configuration Capability.....	294
Figure 8-4. Structure of a Vendor Specific Capability.....	301
Figure 8-5. Structure of a Vendor Specific Extended Capability	301
Figure 8-6. Structure of the Adapter Configuration Space.....	303

Figure 8-7. Basic Configuration Registers of the Adapter Configuration Space	304
Figure 8-8. Structure of the TMU Adapter Configuration Capability	308
Figure 8-9. Structure of the Lane Adapter Configuration Capability.....	311
Figure 8-10. Structure of USB4 Port Capability	314
Figure 8-11. Structure of USB3 Adapter Configuration Capability	320
Figure 8-12. Structure of DP IN Adapter Configuration Capability	323
Figure 8-13. Structure of DP OUT Adapter Configuration Capability	330
Figure 8-14. Structure of PCIe Adapter Configuration Capability.....	335
Figure 8-15. Structure of Path 0 Entry Configuration Space.....	336
Figure 8-16. Structure of Path Entry 'n' in Path Configuration Space at Lane Adapter	337
Figure 8-17. Structure of Path Entry 'n' in Path Configuration Space of a Protocol Adapter	339
Figure 8-18. Configuration of a Path.....	342
Figure 8-19. Structure of the Counters Configuration Space	343
Figure 8-20. Get Capabilities Operation Data Response for Capability Index 0	356
Figure 9-1. LFPS Tunneled Packet Format	386
Figure 9-2. Ordered Set Tunneled Packet Format.....	389
Figure 9-3. Link Command Tunneled Packet Format	390
Figure 9-4. Tunneled ITP Packet Format	391
Figure 9-5. Structure of an Unsegmented USB3 Data Packet	392
Figure 9-6. Segmentation of a USB3 Data Packet.....	393
Figure 9-7. Bandwidth Negotiation by the Internal Host Controller	395
Figure 9-8. Bandwidth Negotiation by the Connection Manager	396
Figure 10-1. DP Adapter Protocol Stack Layers	401
Figure 10-2. DP Adapter State Machine.....	402
Figure 10-3. DP Adapter Path Directions	405
Figure 10-4. DP Stream Resource Mapping Examples.....	407
Figure 10-5. AUX Channel Framing	409
Figure 10-6. AUX Packet Format	409
Figure 10-7. AUX Packet Example.....	410
Figure 10-8. HPD Packet Format.....	411
Figure 10-9. SET_CONFIG Packet Format	411
Figure 10-10. ACK Packet Format	415
Figure 10-11. Power On to HPD Sequence.....	416
Figure 10-12. Target AUX Transaction Flow	421
Figure 10-13. Snoop AUX Transaction Flow	422
Figure 10-14. DP IN Adapter AUX Handling State Machine	424
Figure 10-15. AUX Timing	427
Figure 10-16. Example DP Source Discovery Sequence	429
Figure 10-17. DP Link Training – LTPR CR_DONE.....	434
Figure 10-18. DP Link Training – LTPR – EQ Phase.....	435
Figure 10-19. DP Link Training – DPRX – CR_DONE Phase	436

Figure 10-20. DP Link Training – DPRX – EQ Phase	437
Figure 10-21. Main-Link SST Stream to Tunneled Packets	442
Figure 10-22. TU Set Packing for a 4-Lane Main-Link.....	443
Figure 10-23. TU Set Packing for a 2-Lane Main-Link.....	444
Figure 10-24. TU Set Packing for a 1-Lane Main-Link.....	445
Figure 10-25. EOC Symbol Packing Example	446
Figure 10-26. TU Set Header Format.....	446
Figure 10-27. Video Data Packet Format	448
Figure 10-28. MSA Header Format	448
Figure 10-29. MSA Packet Format.....	449
Figure 10-30. Blank Start Header Format	450
Figure 10-31. Blank Start Packet Format	451
Figure 10-32. Secondary TU Header Format	452
Figure 10-33. Tunneled Secondary Data Path Format	454
Figure 10-34. Secondary Data to Secondary TUs Examples	455
Figure 10-35. Non-Secondary Data Packet Fill Count Examples	457
Figure 10-36. Secondary Data Packet Fill Count Examples	458
Figure 10-37. Sub-MTP TU Structures.....	459
Figure 10-38. Sub-MTP TU Header Format	459
Figure 10-39. Sub-MTP TU 4-Lane Mapping.....	463
Figure 10-40. Sub-MTP TU 2-Lane Mapping.....	463
Figure 10-41. Sub-MTP TU 1-Lane Mapping.....	464
Figure 10-42. Unallocated Sequence, 1-Lane	464
Figure 10-43. Shifting SR, 1-Lane	465
Figure 10-44. ACT Sequence, 1-Lane.....	465
Figure 10-45. SF and VCPF Sequence 4-Lane	466
Figure 10-46. MST Packet Format	467
Figure 10-47. FEC_DECODE Packet Format.....	469
Figure 10-48. FEC Command Format	469
Figure 10-49. Active Video to Blanking	470
Figure 10-50: Adjust PLL Event Occurrence	472
Figure 10-51. Lifetime Counter Format	473
Figure 10-52. Filtered Lifetime Counter Logic Concept	474
Figure 10-53. DP Clock Sync Packet Format	475
Figure 10-54. DP Clock Sync Packet Example.....	476
Figure 10-55: DP IN Adapter Interaction with DPTX During DP BW Allocation	480
Figure 10-56: DP BW Allocation Interaction with Connection Manager.....	482
Figure 11-1. Tunneled PCIe TLP	486
Figure 11-2. Tunneled PTM Example.....	487
Figure 11-3. Tunneled PCIe DLLP	488
Figure 11-4. PCIe DLLP and TLP Tunneled Packet Payload	489
Figure 11-5: Example of PTM Relationships	496

Figure 11-6: PTM ResponseD Message.....	497
Figure 11-7: TMU to PTM Parameters Illustration	499
Figure 12-1. Segmentation of a Frame	504
Figure 12-2. Example of Forwarding an E2E Credit Grant Packet	506
Figure 12-3. E2E Credit Grant / Sync Packet Format	506
Figure 12-4. Transmit Descriptor Structure	510
Figure 12-5. Receive Descriptor Structure (Posted by Host)	513
Figure 12-6. Receive Descriptor Structure (Posted by Host Interface Adapter Layer).....	514
Figure 12-7. Interrupt Moderation	518
Figure 12-8. Structure of the Interrupt Status Registers	527
Figure 12-9. Structure of the Interrupt Vector Allocation Registers (IVAR)	530
Figure 12-10. Structure of the Receive Ring Vacancy Control Register.....	531
Figure 13-1. Bidirectional Re-timer Topology	533
Figure 13-2. Bounce Mechanism	535
Figure 13-3. Structure of the Vendor Specific 1 Capability	548
Figure 13-4. Structure of the Vendor Specific 3 Capability	553
Figure 13-5. Structure of the Vendor Specific 4 Capability	555
Figure 13-6. Structure of the Vendor Specific Extended 6 Capability	556
Figure 13-7. Example Vendor Specific Extended 6 Capability	557
Figure 13-8. Structure of the Common Region	557
Figure 13-9. Structure of a USB4 Port Region	559
Figure 13-10. DP IN Adapter Link Training State Machine	568
Figure 13-11. DP OUT Adapter Link Training State Machine	569
Figure 13-12. Example of a USB4-Based Dock with an Internal Host Controller.....	571
Figure A-1. Examples of Transport Layer Packet HEC Calculation.....	572
Figure A-2. Examples of USB3 Tunneling Calculations	580
Figure A-3. Example of a Credit Grant Record	585
Figure A-4. Example of an HPD Packet Payload	585
Figure A-5. Example of a SET_CONFIG Packet Payload	585
Figure A-6. Example of TU Set Header	586
Figure A-7. Example of a Sub-MTP TU Header.....	586
Figure A-8. Example of an E2E Credit Sync Packet Payload	586
Figure C-1. Successful Entry to CL2 State.....	588
Figure C-2. Successful Entry to CL0s State	588
Figure C-3. Failure to Enter CL2 State.....	589
Figure C-4. Concurrent Requests to Enter CL2 State.....	590
Figure C-5. Error in CL2_REQ Ordered Sets	591
Figure C-6. CL2_REQ Ordered Sets are Partially Received.....	591
Figure C-7. Errors in CL2_REQ Reception and CL_NACK Response.....	592
Figure C-8. Error in CL2_ACK Ordered Sets.....	593
Figure C-9. Error in CL_OFF Ordered Sets.....	593
Figure C-10. CL0s Exit	595

Figure C-11. CL2 (or CL1) Exit 597
 Figure D-1. Pulse Width Modulation 599
 Figure D-2. Serial Time Link Packet Structure 599
 Figure D-3. Serial Time Link Packet Format 600
 Figure D-4. TMU_CLK_OUT and TMU_CLK_IN Parameters 601
 Figure D-5. Definition of TCO_{JTR} 602

Tables

Table 1-1. Rsvd Value and Field Handling 44
 Table 3-1. SBTX and SBRX Specifications 81
 Table 3-2. Electrical Compliance Test Points 83
 Table 3-3. Transmitter Specifications Applied for All Speeds (at TP2) 88
 Table 3-4. Transmitter Frequency Variation Limits During Link Training Before
 Obtaining Steady-State 89
 Table 3-5. Transmit Equalization Presets 93
 Table 3-6. Gen 2 Transmitter Specifications at TP2 95
 Table 3-7. Gen 2 Transmitter Specifications at TP3 96
 Table 3-8. Gen 3 Transmitter Specifications at TP2 97
 Table 3-9. Gen 3 Transmitter Specifications at TP3 98
 Table 3-10. Common Receiver Specifications at TP3' 98
 Table 3-11. Stressed Signal for Gen 2 Receiver Compliance Testing 103
 Table 3-12. Stressed Signal for Gen 3 Receiver Compliance Testing 103
 Table 3-13. Wireless Band Conducted Limits (at TP3) 105
 Table 3-14. Captive Device Transmitter Specifications at TP3 Applied for All Speeds 106
 Table 3-15. Captive Device Transmitter Specifications at TP3 for Gen 2 Systems 107
 Table 3-16. Captive Device Transmitter Specifications at TP3 for Gen 3 Systems 108
 Table 3-17. Common Receiver Specifications at TP2 109
 Table 3-18. Stressed Receiver Conditions for Gen 2 Captive Device Compliance
 Testing (at TP2) 111
 Table 3-19. Stressed Receiver Conditions for Gen 3 Captive Device Compliance
 Testing (at TP2) 111
 Table 3-20. LFPS Electrical Specifications 113
 Table 3-21. RX Margining Voltage and Timing Requirements 116
 Table 3-22. Optional RX Margining Voltage Capabilities 118
 Table 4-1. LT Transaction Format 121
 Table 4-2. LSE Symbol 121
 Table 4-3. AT Transaction Format 122
 Table 4-4. STX Symbol for an AT Transaction 122
 Table 4-5. Broadcast RT Transaction Format 123
 Table 4-6. STX Symbol for a Broadcast RT Transaction 123
 Table 4-7. Contents of Byte 2 in a Broadcast RT Transaction 123
 Table 4-8. Contents of Byte 3 in a Broadcast RT Transaction 124

Table 4-9. Addressed RT Transaction Format.....	124
Table 4-10. STX Symbol for an Addressed RT Transaction	125
Table 4-11. Sideband Channel Receive Transaction State Machine.....	128
Table 4-12. AT/RT Command Data Symbols.....	129
Table 4-13. AT/RT Response Data Symbols.....	129
Table 4-14. Processing of a Received AT/RT Command.....	129
Table 4-15. SB Registers.....	132
Table 4-16. SB Register Fields Access Types	132
Table 4-17. SB Register Fields	132
Table 4-18. Lane Attributes	139
Table 4-19. Transmitter Behavior in Training Sub-states	146
Table 4-20. Training Sub-State Machine Transitions.....	146
Table 4-21. SLOS1 (64b/66b Encoding).....	148
Table 4-22. SLOS2 (64b/66b Encoding).....	149
Table 4-23. SLOS1 (128b/132b Encoding).....	150
Table 4-24. SLOS2 (128b/132b Encoding).....	151
Table 4-25. TS1 and TS2 Ordered Sets	151
Table 4-26. Transmitter Behavior in Bonding Sub-States	153
Table 4-27. Lane Bonding Sub-State Machine Transitions	153
Table 4-28. CL2_REQ Ordered Set	154
Table 4-29. CL1_REQ Ordered Set	155
Table 4-30. CL2_ACK Ordered Set.....	155
Table 4-31. CL1_ACK Ordered Set.....	155
Table 4-32. CL0s_ACK Ordered Set.....	155
Table 4-33. CL_NACK Ordered Set	155
Table 4-34. CL_OFF Ordered Set.....	156
Table 4-35. Ordered Set Structure.....	177
Table 4-36. Scrambling Rules.....	180
Table 4-37. START_RS_FEC Bit Sequence.....	184
Table 4-38. Error Cases and Impact on Logical Layer.....	185
Table 4-39. SKIP Ordered Set.....	186
Table 4-40. De-Skew Ordered Set	187
Table 4-41. TSN Ordered Set	194
Table 4-42. Router State Retained During Sleep	196
Table 4-43. Wake Events	197
Table 4-44. Logical Layer Timing Parameters.....	198
Table 5-1. Transport Layer Packet Header Format	202
Table 5-2. Credit Grant Packet Header.....	205
Table 5-3. Credit Grant Record Format.....	205
Table 5-4. Path Credit Sync Packet Header.....	206
Table 5-5. Path Credit Sync Packet Payload	206
Table 5-6. Shared Buffers Credit Sync Packet Header.....	207

Table 5-7. Shared Buffers Credit Sync Packet Payload	207
Table 5-8. Transport Layer Behavior per Link State	207
Table 5-9. Minimum Transport Layer Header Gap Requirements	208
Table 5-10. Ingress Adapter Flow Control Schemes	216
Table 5-11. Buffer Allocation Parameters	217
Table 5-12. Egress Adapter Flow Control Schemes	221
Table 5-13. Transport Layer Timing Parameters	226
Table 6-1. Control Packet Payload	231
Table 6-2. Content of a Read Request.....	232
Table 6-3. Content of a Read Response	234
Table 6-4. Content of a Write Request.....	235
Table 6-5. Content of a Write Response	237
Table 6-6. Content of a Notification Packet.....	238
Table 6-7. Content of a Notification Acknowledgement Packet.....	239
Table 6-8. Content of a Hot Plug Event Packet.....	239
Table 6-9. Content of an Inter-Domain Request.....	240
Table 6-10. Content of an Inter-Domain Response	241
Table 6-11. Notification Events.....	246
Table 6-12. Configuration Layer Timing Parameters	252
Table 7-1. Bidirectional UFP Timeout Values.....	259
Table 7-2. Bidirectional DFP Timeout Values.....	260
Table 7-3. Follow-Up Packet Payload	267
Table 7-4. Inter-Domain Time Stamp Packet Payload	269
Table 7-5. Definition of Variables.....	270
Table 7-6. Index Notation	270
Table 7-7. Time Synchronization Accuracy Parameters	281
Table 8-1. Configuration Register Fields Access Types	283
Table 8-2. List of Router Configuration Capabilities	285
Table 8-3. Router Configuration Space Basic Attributes	286
Table 8-4. TMU Router Configuration Capability Fields.....	295
Table 8-5. Locked Registers Groups.....	300
Table 8-6. Vendor Specific Capability Fields.....	301
Table 8-7. Vendor Specific Extended Capability Fields	302
Table 8-8. List of Adapter Configuration Capabilities	303
Table 8-9. Adapter Configuration Space Basic Attributes.....	304
Table 8-10. Adapter Types	308
Table 8-11. TMU Adapter Configuration Capability Fields.....	309
Table 8-12. Contents of the Lane Adapter Configuration Capability	311
Table 8-13. USB4 Port Capability Fields.....	315
Table 8-14. USB3 Adapter Configuration Capability Fields	320
Table 8-15. DP IN Adapter Configuration Capability Fields	323
Table 8-16. DP OUT Adapter Configuration Capability Fields	330

Table 8-17. PCIe Adapter Configuration Capability Fields.....	335
Table 8-18. Contents of Path 0 Entry.....	337
Table 8-19. Contents of Path Entry in Path Configuration Space at Lane Adapter.....	338
Table 8-20. Contents of Path Entry in Path Configuration Space of a Protocol Adapter	339
Table 8-21. Counter Set Fields.....	343
Table 8-22. List of Router Operations.....	345
Table 8-23. Query DP Resource Availability Operation Metadata.....	346
Table 8-24. Query DP Resource Availability Completion Metadata and Status.....	346
Table 8-25. Allocate DP Resource Operation Metadata.....	346
Table 8-26. Allocate DP Resource Completion Metadata and Status.....	347
Table 8-27. De-Allocate DP Resource Operation Metadata.....	347
Table 8-28. De-Allocate DP Resource Completion Metadata and Status.....	347
Table 8-29. NVM Set Offset Operation Metadata.....	348
Table 8-30. NVM Set Offset Completion Metadata and Status.....	349
Table 8-31. NVM Write Operation Data.....	349
Table 8-32. NVM Write Completion Status.....	350
Table 8-33. NVM Authenticate Write Completion Status.....	350
Table 8-34. NVM Read Operation Metadata.....	351
Table 8-35. NVM Read Router Completion Metadata.....	351
Table 8-36. NVM Read Router Completion Data.....	351
Table 8-37. DROM Read Router Operation Metadata.....	352
Table 8-38. DROM Read Router Completion Metadata and Status.....	352
Table 8-39. DROM Read Router Completion Data.....	352
Table 8-40. Get NVM Sector Size Completion Metadata and Status.....	353
Table 8-41. Get PCIe Downstream Entry Mapping Completion Metadata and Status.....	354
Table 8-42. Get PCIe Downstream Entry Mapping Completion Data.....	354
Table 8-43. Get Capabilities Operation Metadata.....	355
Table 8-44. Get Capabilities Operation Completion Metadata and Status.....	355
Table 8-45. List of Capabilities.....	356
Table 8-46. Set Capabilities Operation Metadata.....	357
Table 8-47. List of Capabilities.....	357
Table 8-48. Set Capabilities Operation Completion Status.....	357
Table 8-49. Buffer Allocation Request Router Completion Status and Metadata.....	358
Table 8-50. Buffer Allocation Request Router Completion Data DW Structure.....	358
Table 8-51. Get Container-ID Router Completion Status.....	359
Table 8-52. Get Container-ID Router Completion Data DW Structure.....	359
Table 8-53. Block Sideband Port Operation Completion Status.....	359
Table 8-54. Unblock Sideband Port Operation Completion Status.....	360
Table 8-55. List of Port Operations.....	362
Table 8-56. SET_TX_COMPLIANCE Operation Metadata.....	365
Table 8-57. SET_RX_COMPLIANCE Operation Metadata.....	367
Table 8-58. START_BER_TEST Operation Metadata.....	368

Table 8-59. END_BER_TEST Operation Metadata	368
Table 8-60. END_BER_TEST Completion Data	369
Table 8-61. END_BURST_TEST Operation Metadata	370
Table 8-62. END_BURST_TEST Completion Data	370
Table 8-63. READ_BURST_TEST Operation Metadata	371
Table 8-64. READ_BURST_TEST Completion Data	371
Table 8-65. ENTER_EI_TEST Operation Metadata	372
Table 8-66. ROUTER_OFFLINE_MODE Operation Metadata	372
Table 8-67. READ_LANE_MARGIN_CAP Completion Data	374
Table 8-68. RUN_HW_LANE_MARGINING Operation Metadata	376
Table 8-69. Contents Selection for RUN_HW_LANE_MARGINING Completion Data	376
Table 8-70. RUN_HW_LANE_MARGINING Completion Data	377
Table 8-71. RUN_SW_LANE_MARGINING Operation Metadata	380
Table 8-72. RUN_SW_LANE_MARGINING Completion Data	381
Table 8-73. READ_SW_MARGIN_ERR Completion Metadata	382
Table 9-1. PDF Values for USB3 Tunneling Packets	385
Table 9-2. LFPS Tunneled Packet Payload	385
Table 9-3. Ordered Set Tunneled Packet Payload	389
Table 9-4. USB3 Adapter Timing Parameters	396
Table 9-5. USB3 Timers and Timeout Values	397
Table 10-1. DisplayPort Modes Of Operation Over DisplayPort Tunneling	404
Table 10-2. Recommended Path Parameters	405
Table 10-3. DP Stream Resource Allocation Commands	407
Table 10-4. AUX Path Tunneled Packet Types	408
Table 10-5. Main-Link Path Tunneled Packet Types	408
Table 10-6. SET_CONFIG Message	413
Table 10-7. DisplayPort Required Bandwidth (Gbps)	418
Table 10-8. HPD Event Propagation Delay Requirement	420
Table 10-9. DPCD Internal Addresses	423
Table 10-10. DP IN Adapter AUX Handling State Machine	424
Table 10-11. AUX Delay Requirements	427
Table 10-12. Aggregated DisplayPort Capabilities	427
Table 10-13. DP Adapter Operation Mode Transitions	430
Table 10-14. Blank Start Control Link Symbols Mapping	451
Table 10-15. Fill Count Prev_Factor	456
Table 10-16. Slot Zero Sub-MTP TU Header Types	459
Table 10-17. Non-Slot Zero Sub-MTP TU Header Types	460
Table 10-18. Slot Zero Sub-MTP TU Packet Rules	460
Table 10-19. Non- Zero Slot Sub-MTP TU Packet Rules	461
Table 10-20. K-Code Index Nibble in Parameter Byte	462
Table 10-21. FLC Calculation Examples	474
Table 10-22. DPCD Bandwidth Allocation Registers	478

Table 10-23. DP IN Adapter Configuration Space Mapping	479
Table 10-24. DP Adapter Timing Parameters	483
Table 11-1. PDF Values for PCIe Tunneled Packets	485
Table 11-2. TLP Pre-Header.....	487
Table 11-3. TS Ordered Sets	490
Table 11-4. Electrical Idle Ordered Sets	490
Table 11-5. PCIe Link Timer Ranges	495
Table 11-6. PCIe Adapter Timing Parameters.....	500
Table 12-1. Frame Mode Tunneled Packet Format	504
Table 12-2. E2E Credit Grant Packet Header	506
Table 12-3. E2E Credit Grant Packet Payload	506
Table 12-4. E2E Credit Sync Packet Header	507
Table 12-5. E2E Credit Sync Packet Payload	507
Table 12-6. Transmit Descriptor Contents	510
Table 12-7. Receive Descriptor Contents (Posted by Host).....	513
Table 12-8. Receive Descriptor Contents (Posted by Host Interface Adapter Layer)	514
Table 12-9. Access Types	519
Table 12-10. Summary of Memory BAR Registers	519
Table 12-11. Host Interface Capabilities Register	520
Table 12-12. Host Interface Reset Register	521
Table 12-13. Host Interface Control Register	521
Table 12-14. Host Interface CL1 Enable	521
Table 12-15. Host Interface CL2 Enable	521
Table 12-16. Base Address Low Register	522
Table 12-17. Base Address High Register	522
Table 12-18. Producer and Consumer Indexes Register	522
Table 12-19. Ring Size Register	523
Table 12-20. Ring Control Register.....	524
Table 12-21. Base Address Low Register	524
Table 12-22. Base Address High Register	524
Table 12-23. Producer and Consumer Indexes Register	525
Table 12-24. Ring Size Register	525
Table 12-25. Ring Control Register.....	526
Table 12-26. PDF Bit Masks Register	527
Table 12-27. Interrupt Status	528
Table 12-28. Interrupt Status Clear.....	528
Table 12-29. Interrupt Status Set.....	528
Table 12-30. Interrupt Mask.....	529
Table 12-31. Interrupt Mask Clear	529
Table 12-32. Interrupt Mask Set	529
Table 12-33. Interrupt Throttling Rate (ITR).....	529
Table 12-34. Interrupt Vector Allocation (IVAR)	530

Table 12-35. Receive Ring Vacancy Control.....	531
Table 12-36. Receive Ring Vacancy Status	531
Table 12-37. Host Interface Timing Parameters	532
Table 13-1. Thunderbolt 3 Parameters	532
Table 13-2. TBT3 LT Transaction Types.....	534
Table 13-3. STX Symbol.....	534
Table 13-4. Contents of Byte 2 in a Broadcast RT Transaction	535
Table 13-5. SB Registers.....	536
Table 13-6. SB Registers Fields	536
Table 13-7. Lane Attributes	537
Table 13-8. TS1 and TS2 Ordered Set Structure	542
Table 13-9. Router State Retained During Sleep	543
Table 13-10. Logical Layer Timing Parameters	544
Table 13-11. Buffer Allocation by TBT3 Connection Manager	545
Table 13-12. Configuration Register Fields Access Types	548
Table 13-13. List of TBT3-Compatible Router Configuration Capabilities	548
Table 13-14. Vendor Specific 1 Capability Fields	549
Table 13-15. Vendor Specific 3 Capability Fields	553
Table 13-16. Vendor Specific 4 Capability Fields	555
Table 13-17. Common Region Fields.....	557
Table 13-18. USB4 Port Region Fields	559
Table 13-19. Adapter Configuration Space Basic Attributes	563
Table 13-20. USB4 Port Capability Fields	564
Table 13-21. DP IN Adapter Link Training State Machine Transition Table	568
Table 13-22. DP OUT Adapter Link Training State Machine Transition Table.....	569
Table A-1. Examples of Control Packet CRC Calculation.....	573
Table A-2. Example of a Read Command	573
Table A-3. Example of a Write Command	573
Table A-4. Examples of Scrambler Computations	574
Table A-5. Example 1 – RS-FEC Block.....	574
Table A-6. Example 2 – RS-FEC Block.....	576
Table A-7. Example 3 – RS-FEC Block.....	577
Table A-8. Example 4 – RS-FEC Block.....	578
Table B-1. Transport Layer Packet Summary.....	586
Table D-1. Serial Time Link Packet Fields	600
Table D-2. TMU_CLK_OUT and TMU_CLK_IN Specifications.....	602

1 Introduction

1.1 Scope of the Document

The specification is primarily targeted at peripheral developers and platform/adaptor developers, but provides valuable information for platform operating system/BIOS/device driver, adaptor independent hardware vendors/independent software vendors, and system OEMs. This specification can be used for developing new products and associated software.

1.2 USB Product Compliance

Adopters of the USB4™ specification have signed the USB4 Adopters Agreement, which provides them access to a royalty-free reasonable and nondiscriminatory (RAND) license from the Promoters and other Adopters to certain intellectual property contained in products that are compliant with the USB4 specification. Adopters can demonstrate compliance with the specification through the testing program as defined by the USB Implementers Forum (USB-IF). Products that demonstrate compliance with the specification will be granted certain rights to use the USB-IF logos as defined in the logo license.

1.3 Document Organization

Chapters 1 and 2 provide an overview for all readers, while Chapters 3 through 13 contain detailed technical information defining USB4.

1.4 Design Goals

USB 3.1 and USB 3.2 were evolutionary steps to increase bandwidth. The goal for USB4 remains the same with the added goal of helping to converge the USB Type-C® connector ecosystem and minimize end-user confusion. Several key design areas to meet this goal are listed below:

- Offer display, data, and load/store functionality over a single USB Type-C connector.
- Retain compatibility with existing ecosystem of USB and Thunderbolt™ products.
- Define Port Capabilities for predictable and consistent user experience.
- Provide increased host flexibility to configure bandwidth, power management, and other performance-related parameters for system needs.

1.5 Related Documents

Universal Serial Bus 3.2 Specification, Revision 1.0, September 22, 2017 (USB 3.2 Specification)

USB Type-C® Cable and Connector Specification, Release 2.0 (USB Type-C Specification)

USB 3.0 Jitter Budgeting white paper (USB Jitter Paper)

Universal Serial Bus Power Delivery Specification, Release 3.0, Version 2.0, August 2019 (USB PD Specification)

PCI Express® Base Specification, Revision 4, Version 1, September 27, 2017 (PCIe Specification)

VESA DisplayPort™ Standard, Revision 1.2a, May 2012 (DisplayPort 1.2a Specification)

VESA DisplayPort™ Standard, Revision 1.4a, April 19, 2018 (DisplayPort 1.4a Specification)

VESA DisplayPort™ 1.4a PHY Layer Compliance Test Specification, Revision 1.0, 27 July, 2018 (DisplayPort 1.4a PHY CTS)

VESA DisplayPort™ Alt Mode on USB Type-C Standard, Revision 1.0b, November 03, 2017 (DisplayPort Alt Mode Specification)

eXtensible Host Controller Interface for Universal Serial Bus, Revision 1.1 (xHCI Specification)

USB4 Connection Manager (CM) Guide, Revision 1.0, [to be published] – (Connection Manager Guide)

USB4 Re-Timer Specification, [to be published] – (USB4 Re-Timer Specification)

USB4 Device ROM (DROM) Specification, Revision 1.0, [to be published] – (USB4 DROM Specification)

USB4 Inter-Domain Specification, Revision 1.0, [to be published] – (USB4 Inter-Domain Specification)

HDCP on DisplayPort™ Specification, Revision 2.3, January 22, 2019 (HDCP Specification)